VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

1. (Twice Amended) A multi-chip module system comprising:

a substrate having at least a first position having, in turn, a predetermined configuration for locating a first semiconductor device thereat and having at least one other vacant position having, in turn, a predetermined configuration for locating a second semiconductor device thereat on the multi-chip module system; and

a first semiconductor device located in the at least first position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; said first semiconductor device being burned in at said location on said substrate.

2. (Two Times Amended) The multi-chip module system of claim 1, further comprising:

the at least one other vacant position having the predetermined configuration for locating the second semiconductor device thereat which is substantially the same as the predetermined configuration of the first [semiconductor device] position.

5. (Twice Amended) A multi-chip module system comprising:

a substrate having a first position having, in turn, a predetermined configuration for locating a first semiconductor device thereat, having a second position having, in turn, a predetermined configuration for locating a second semiconductor device thereat, and having at least one other vacant position having, in turn, a predetermined configuration for locating a third semiconductor device thereat on the multi-chip module system;

the first semiconductor device located in the first position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and

the second semiconductor device located in the second position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic; said first and second semiconductor devices being burned in at said first and second positions, respectively, on said substrate.

6. (Two Times Amended) The multi-chip module system of claim 4, further comprising:

the at least one other vacant position having a predetermined configuration for locating a third semiconductor device thereat which is substantially the same as the predetermined configuration of the first [semiconductor device] position.

17. (Twice Amended) A multi-chip module system comprising:

a substrate having a first position having, in turn, a predetermined configuration for locating a first semiconductor device thereat, having a second position having, in turn, a predetermined configuration for locating a second semiconductor device thereat, having a first vacant position having, in turn, a predetermined configuration for locating a third semiconductor device thereat, and having a second vacant position having, in turn, a predetermined configuration for locating a fourth semiconductor device thereat on the multi-chip module system;

the first semiconductor device located in the first position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and

the second semiconductor device located in the second position of the substrate for use in the multi-chip module system, the second semiconductor device having a second

predetermined performance characteristic; said first and second semiconductor devices being burned in at said first and second positions, respectively, on said substrate.

18. (Two Times Amended) The multi-chip system module of claim 17, wherein:
at least a portion of said substrate is substantially sheet-like, and wherein the first vacant position is located on the side of the substrate which is opposite the [located on one] side [of the substrate] upon which [; and] the second vacant position [on the substrate] is located [on the other side of the substrate].

19. (Twice Amended) A multi-chip module system comprising:
a substrate having at least a first predetermined configuration position for locating a first semiconductor device thereat and having at least one other vacant predetermined configuration position for locating a second semiconductor device thereat on the multi-chip module system; and
the first semiconductor device located in the at least the first predetermined configuration position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; said first semiconductor device being burned in at said first predetermined configuration position on said substrate.

20. (Two Times Amended) The multi-chip module system of claim 19, further comprising:
the at least one other vacant predetermined configuration position for locating the second semiconductor device thereat which is substantially the same as the predetermined configuration of the first [semiconductor device] position.

23. (Two Times Amended) A multi-chip module system comprising:

a substrate having a first predetermined configuration position for locating a first semiconductor device thereat, having a second predetermined configuration position for locating a second semiconductor device thereat, and having at least one other vacant predetermined configuration position for locating a third semiconductor device thereat on the multi-chip module system;

the first semiconductor device located in the first predetermined configuration position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and

the second semiconductor device located in the second predetermined configuration position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic; wherein said first and second semiconductor devices being burned in at said first and second predetermined configuration positions, respectively, on said substrate.

24. (Two Times Amended) The multi-chip module system of claim 23, further comprising:

the at least one other vacant predetermined configuration position for locating the third semiconductor device thereat which is substantially the same as the predetermined configuration of the first [semiconductor device] position.

35. (Two Times amended) A multi-chip module system comprising:

a substrate having a first predetermined configuration position for locating a first semiconductor device thereat, having a second predetermined configuration position for locating a second semiconductor device thereat, having a first vacant predetermined configuration position for locating a third semiconductor device thereat, and having a second vacant

predetermined configuration for locating a fourth semiconductor device thereat on the multi-chip module system;

the first semiconductor device located in the first predetermined configuration position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and

the second semiconductor device located in the second predetermined configuration position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic; said first and second semiconductor devices being burned in at said first and second predetermined configuration positions, respectively, on said substrate.

36. (Two Times Amended) The multi-chip system module of claim 35, wherein:

at least a portion of said substrate is substantially sheet-like, and wherein the first vacant predetermined configuration position is located on the side of the substrate which is opposite the [located on one] side [of the substrate] upon which [and]) the second vacant predetermined configuration position [on the substrate] is located [on the other side of the substrate].